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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,416	06/12/2001	Ian M. Flanagan	L13.12-0157/01-191	4140

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EXAMINER	
ETTEHADIEH, ASLAN	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,416	FLANAGAN ET AL.	
	Examiner	Art Unit	
	Aslan Ettehadieh	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 - 17* is/are allowed.

6)☒ Claim(s) *1,6, and 18* is/are rejected.

7)☒ Claim(s) *2-5 and 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawing

The drawings are objected to under 37 CFR 1.83(a) because they fail to show *where element 50 is in reference to on the drawing (figure 1 element 50)* as described in the specification (page 8 line 7). Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 1, 6, and18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11 and 12 of U.S. Patent No. 6262634 in view of Lin (US 6868504).

2. Regarding claim 1, Flanagan discloses a method of measuring phase margin phase-locked loop (PLL) having a reference input, the method comprising (claim 1):

(a) applying a reference the reference input (claim 1);

(b) providing an auxiliary variable delay within the PLL (claim 1, where auxiliary variable delay in being interpreted as variable delay);

(c) varying the auxiliary variable delay until the PLL becomes unstable (claim 1, where auxiliary variable delay in being interpreted as variable delay and varying is being interpreted as increasing); and

(d) generating a phase margin output related the phase margin as a function of value the auxiliary variable delay which PLL becomes unstable (claim 1, where auxiliary variable delay in being interpreted as variable delay). Flanagan does not disclose a DLL.

In the same field of endeavor, however, Lin discloses a DLL (col 1 lines 22 – 45).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a DLL as taught by Lin in the system of Flanagan's phase margin testing.

Applicant has not disclosed that a DLL provides an advantage, is used for a particular purpose or solves a stated problem.

One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a DLL because a PLL and a DLL both provide synchronization.

Therefore, it would have been obvious to combine to one of ordinary skill in this art to modify the PLL with a DLL to obtain the invention as specified in the claim.

3. Regarding claim 6, Flanagan discloses all limitations of claim 6 as analyzed in claim 1 above. Flanagan further discloses wherein:

step (b) comprises providing an analog voltage-controlled delay element within PLL, which has a control voltage input (claim 12, where analog voltage-controlled delay element is being interpreted as a voltage-controlled delay element); and

step (c) comprises applying control voltage the control voltage input and varying control voltage (claim 12, where control voltage is being interpreted as voltage and varying is being interpreted as increasing). Flanagan does not disclose a DLL.

In the same field of endeavor, however, Lin discloses a DLL (col 1 lines 22 – 45).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a DLL as taught by Lin in the system of Flanagan's phase margin testing.

Applicant has not disclosed that a DLL provides an advantage, is used for a particular purpose or solves a stated problem.

One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a DLL because a PLL and a DLL both provide synchronization.

Therefore, it would have been obvious to combine to one of ordinary skill in this art to modify the PLL with a DLL to obtain the invention as specified in the claim.

4. Regarding claim 18, Flanagan discloses a phase-locked loop (PLL) comprising:

a reference input for receiving reference signal (claim 20, where it is inherent that a reference input is for receiving reference signal);

a feedback input for receiving a feedback signal (claim 20, where a loop coupled between the reference input and the output provides a feedback signal and where it is inherent that a feedback input is for receiving a feedback signal);

a PLL output coupled to feedback input (claim 20);

phase control means detecting phase difference between the reference signal and the feedback signal and for varying the first variable delay as a function of the phase difference (claim 20); and

phase margin measurement means for adding further delay series with the variable delay means, between the reference input and the feedback input, and generating a phase margin output as function an amount of the further delay that is required for the PLL to become unstable (claim 20, where introducing delay is being interpreted as adding further delay). Flanagan does not disclose a DLL and a first variable delay means coupled between the reference input and the DLL output for providing a first variable delay.

In the same field of endeavor, however, Lin discloses a DLL (col 1 lines 22 – 45) and a first variable delay means (figure 6 element 84) coupled between the reference input (figure 6 element CLKref) and the DLL output (figure 9 element Out) for providing a first variable delay (figure 6 element 84).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a DLL as taught by Lin in the system of Flanagan's phase margin testing.

Applicant has not disclosed that a DLL provides an advantage, is used for a particular purpose or solves a stated problem.

One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a DLL because a PLL and a DLL both provide synchronization.

Therefore, it would have been obvious to combine to one of ordinary skill in this art to modify the PLL with a DLL to obtain the invention as specified in the claim.

Furthermore, it would have been obvious to one skilled in the art at the time of invention was made to use a first variable delay means coupled between the reference input and the DLL output for providing a first variable delay as taught by Lin in the system of Flanagan's phase margin testing to improve tracking in order to provide for better efficiency.

Allowable Subject Matter

5. Claims 2 – 5 and 7 – 10 are objected to as being dependent upon a rejected base claim, but would be allowable if the double patenting rejection above is overcome.

6. Claims 11 – 17 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art fails to teach or suggest, alone or in combination, a method of measuring phase margin of a DLL circuit, where the auxiliary variable delay of the DLL circuit is varied until the DLL is unstable and to generate a phase margin output

associated with delay when the DLL is unstable as recited in claim 11 and in combination with other elements of the claims.

Other prior art cited

The prior art made of record and not relies upon is considered pertinent to applicant's disclosure.

8. Harrison (US 6173432) discloses a DLL circuit that includes multiple delays, phase detector, reference input, a delayed output, a feedback loop, charge pump, and a multiplexer.

9. Funaba (US 6212127) discloses a DLL circuit that includes a variable delay circuit, delay circuit, phase comparator, reference input, an output, and a feedback loop.

10. Pyeon et al. (US 6392456) discloses a DLL circuit that includes a variable delay circuit, delay circuit, phase detector, charge pump, multiplexer, reference input, an output, and a feedback loop.

11. Jefferson et al. (US 5963069) discloses a DLL circuit that includes a variable delay circuit, delay circuit, phase detector, counter, reference input, an output, and a feedback loop.

12. Konno (US 5828250) discloses a DLL circuit that includes an adjustable delay line, delay line, phase detector, multiplexer, reference input, an output, and a feedback loop.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aslan Ettehadieh whose telephone number is (571) 272-8729. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aslan Ettehadieh
Examiner
Art Unit 2637

AE

JAY K. PATEL
SUPERVISORY PATENT EXAMINER